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FLOATING ADC METHOD* FOR SERIES – PARALLEL A/D CONVERSION

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ABSTRACT

In this paper, a fully integrable 8 bit series-parallel AD converter based on a new "floating ADC" principle is presented.

Cross-plot testst of the experimental converter revealed that the differential nonlinearity of the 8 bit system will be less than $\pm \frac{1}{4}$ *LSB for an analog input voltage of* fV_{pp}.

A converter of this type provides a good alternative to the all parallel system at sampling frequencies up to 100 MHz, when chip size and power dissipation must be reduced.

INTRODUCTION

Several problems arise when attempting to apply the concept of series-parallel AD conversion to achieve the greater resolution required for wordlength of 8 bit, at the sampling rate of 100 MHz 1.

First of all, the accuracy of the system is mainly determined by the DAC used in the circuit. Moreover, the circuits which drive the differential amplifier (Dif. A.) through the (+) and (−) inputs, respectively, are not identical and result in a temperature dependent offset voltage at the output of the amplifier. This offset voltage causes a considerable error degrading the overall accuracy of the ADC (Fig. 1).

On the other hand, digital sampling can be applied with the use of latched comparators to increase the conversion speed to the 100 MHz range which cannot be offered by the available sample and hold circuits. In this case there is no need for a high speed and high accuracy sample and hold circuit but one needs a high precision analog delay circuit in order to compensate for the signal transmission delay in the first ADC and DAC, i.e. $(T_1 + T_2)$, (Fig. 1).

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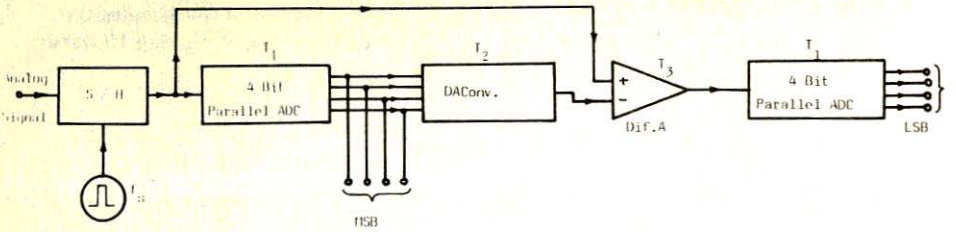

Fig. 1 – Series-parallel converter with the sample and hold circuit

In bipolar technology, it is quite difficult to realize such an analog delay circuit giving precisely the delay of $(T_1 + T_2)$ within the desired bandwidth.

Thus, to eleminate this delay circuit and solve the offset problem of the differential amplifier, a new "Floating ADC" principle is developed and applied.

THE FLOATING ADC PRINCIPLE

In this series-parallel conversion principle the second ADC is floating over the intervals between the quantization levels of the first ADC (Fig. 2), and is connected to the appropriate interval corresponding to the momentary value of the analog input signal without waiting for the appearance of the MSB output. It will be seen that no additional analog delay-circuit is necessary for signals commonly encountered in practice, when the determination of the interval and the connection of the second ADC is realized with sufficiently fast circuitry.

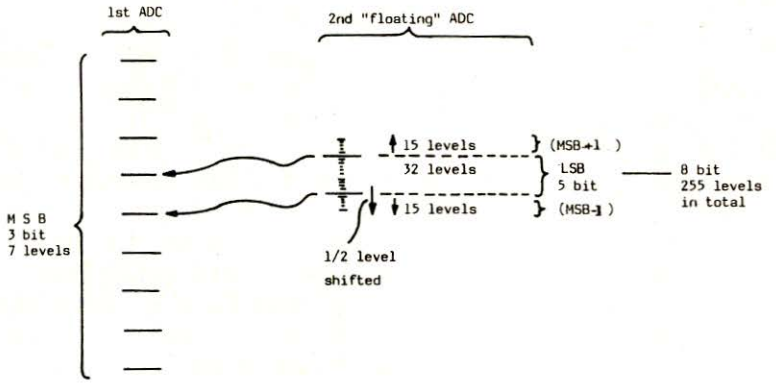

Fig. 2 – The "floating ADC" principle applicable in series-parallel conversion method

The block diagram of the new series-parallel ADC based on the "Floating ADC" principle is given in Fig. 3, where the first ADC (Center block) which is a fully parallel digitally sampled 3 bit device, differs from a conventional one only in that it incorporates a (± 1) circuit.

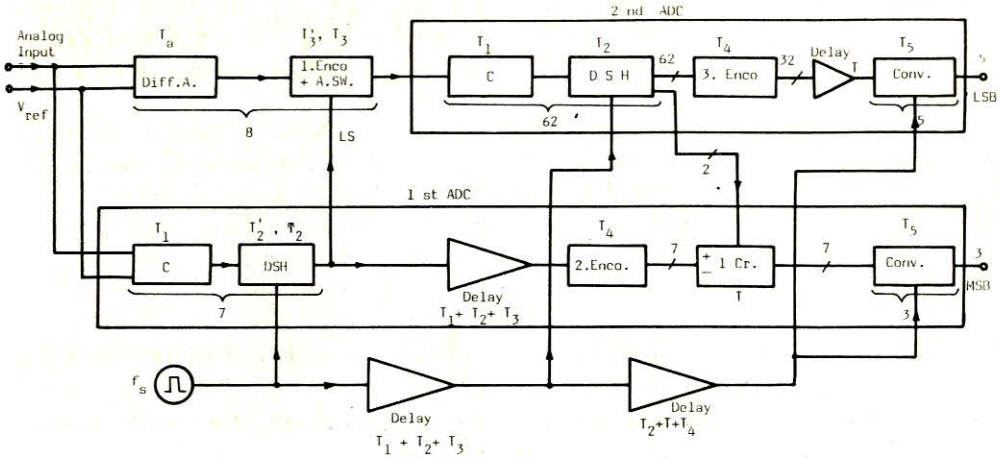

Fig. 3 – Block diagram of the new series-parallel ADC based on the "floating ADC" principle

The second ADC (upper block) is also a digitally sampled 5-bitparallel converter having (± 1) command outputs. This converter has additional 15 levels above and below the normal 32 Levels, respectively. These 62 levels are combined in such a way as to result into normal 5-bit LSB at the output of the converter (Fig. 2 and 3). Second ADC encoding levels are given in Fig. 4 where (± 1) command levels are indicated.

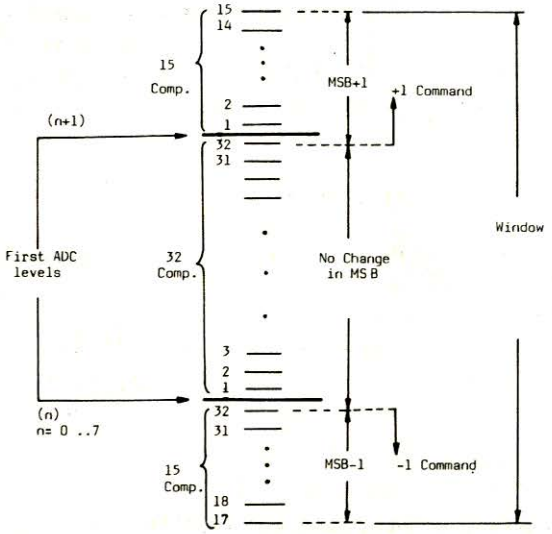

Fig. 4 – 2 nd ADC encoding levels

The blocks which deliver the input signal of the 2 nd. ADC (input connection circuits of the 2 nd. ADC), Fig. 3, exhibit following significant differences in comparison with the system in Fig. 1:

i.— The inputs of the 2 nd. ADC driving blocks (Fig. 3) are parallel with inputs of 1 st. ADC, so that they are both fed by the same analog and 7 reference voltages, which give an equally spaced 7 value scale (0—7).

ii.— The 2 nd. ADC driving blocks consist of 8-differential amplifiers and 8-"1 st Encoder + analog switch" circuits, each corresponding to one quantization level (encoding level) of the 1 st. ADC (from zero to seven).

iii.— The analog switches can be realized in a differential form which results in a less temperature dependent offset voltage than that of the unsymmetrically driven differential amplifier "Dif. A" of Fig. 1.

iv.— Logic input signals (LS) of the 1 st. encoder circuits which activate their analog switches are delivered by the 7-outputs of the latched comparators (C + DSH) of the 1 st. ADC.

That gives the possibility to control the analog switches without waiting until the 3 bit MSB value becomes available at the output.

The encoding levels of the 1 st and 2 nd ADC's are given in Fig. 2. Second ADC encoding levels are redrawn in Fig. 2 in detail.

The logic output signals from seven (C + DSH) blocks of the 1 st. ADC give a coarse representation of the analog input voltage: All blocks with reference voltages below the input voltage produce a logic "1". That information is used both by the 1 st. and 2 nd. encoders (Fig. 3) to determine the level which is passed by the analog input signal.

At the same time, all differences between the analog signal and the reference voltage levels (0 — 7) are available at the outputs of the differential amplifiers (Dif. A). As soon as the 1 st. encoder activates the correct analog switch corresponding to the level passed, the related difference is immediately applied to the input of the 2 nd. In other words, the 2 nd. ADC is connected to the appropriate window determined by the instantaneous value of the analog input signal. Evidently the 2 nd. ADC is a "Floating ADC" and hence this technique can be called as the "Floating ADC" method.

EXPERIMENTAL 6 BIT CONVERTER

An experimental 6 Bit ADC has been built consisting of two cards, one containing the 3 bit "1 st. ADC" and "input connection circuit of the 2 nd. ADC", the second containing the 3 bit "2 nd. ADC".

The complete circuitry has been realized using Schottky TTL comparators: 25 X (NE 529 N); transistor arrays: 15 X (CA 3127 E), 4 X (CA 3046), 4 X (CA 3102), JK flip-flops: 8 X (74S112) and NAND gates: 9 X (74S00), 7 X (74S10).

TESTING

By superimposing a triangular-wave signal (V_{ac}) on a dc. voltage (V_{dc}) applied to the input of the ADC under test, we can sweep some of the ADC output

codes of interest on the oscilloscope screen (Fig. 5).

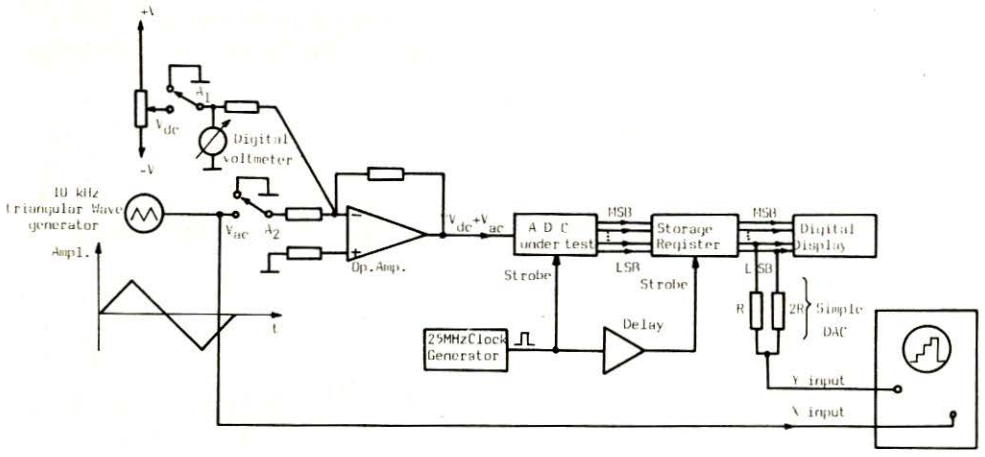

Fig. 5 — Set-up for the dynamic cross-plot test

Using a dynamic cross-plot test the set-up of Fig. 13 enables us to determine the analog values corresponding to the transitions and the center of each code quantization level, which in turn permits determining device nonlinearity and differential nonlinearity. For this purpose, the two least significant bits are decoded by a simple R-2R DAC. This decoded signal is fed to the vertical input of the oscilloscope while the triangular-wave signal is applied to the horizontal input of the scope.

The experimental 6 bit ADC has been tested and results of the cross-plot test are as follows:

i.— There was no missing code through the whole analog input range.

ii.— Transfer characteristic was completely monotonic.

iii.— With a 1 V_{pp}, 10 kHz triangular-wave input signal at 25 MHz sampling rate, maximum differential nonlinearity was found to be 0,1 LSB.

CONCLUSIONS

1 — A maximum differential nonlinearity of 0,1 LSB permits to increase the number of the 2 nd. ADC bits from 3 to 5 in order to have an 8 bit converter. In this case it can be estimated that the differential nonlinearity will not be greater than 0,4 LSB giving an acceptable S/N ratio for an 8 bit ADC. On the other hand, if an analog input signal of 2 V_{pp} is used, differential nonlinearity further reduces to 0,2 LSB resulting in a better S/N ratio.

2 — If a high speed bipolar process is applied (f_T = 3 GHz for I_E = 1mA), the integrated 8 bit ADC can easly operate at a sample rate of 100 MHz owing to the high speed of the ECL mode circuitry used.

3 — There is no need for a precise analog delay circuit in the device.

4 — Although the number of quantization levels of the 2 nd. ADC is increased to avoid the use of an analog delay circuit, it can be said that the circuitry offers a considerable reduction in the number of circuit elements as compared with an 8 bit all parallel device (255 to 69 circuit units).

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